REMARKS

In paragraph 2 of the Office action, the drawings are objected to under 37 CFR 1.83(a) for allegedly failing to show every feature of the invention specified in the claims. The examiner indicated that the "peripheral devices including controllers must be shown or the feature(s) cancelled from the claims(s)". The phrase "peripheral devices" has been removed from the claims. Accordingly, the objection to the drawings has been rendered moot by the amendment to the claims.

In paragraph 5 of the Office action, claims 43 - 48 are rejected under 35 U.S.C. §112, first paragraph, because the specification "while being enabling for the processor access [sic] the memory arrays, does not reasonably provide enablement for a plurality of peripheral devices writing and reading information out of the memory cells with the peripheral devices including a plurality of controllers connected to the memory banks." The peripheral circuits (devices) are discussed in paragraphs 38 and 57 of the application. However, to advance the prosecution of this application, the phrase "peripheral devices" has been replaced in the claims with the word "circuits". It is applicant's position that the specification, written for a person of ordinary skill in the art, is enabling with respect to the circuits needed for writing information into and reading information out of the memory cells. Applicant respectfully requests that the rejection of claims 43 - 48 under 35 U.S.C. §112, first paragraph, be withdrawn.

Claims 1 - 10 have been cancelled. Accordingly, no response is needed with respect to paragraphs 9 and 10 of the Office action.

In paragraph 11 of the Office action, claim 11 stands rejected in view of Nakamura, specifically Figure 2, paragraphs 0056 - 0061. It is the Office's position that "Figure 2 shows each memory bank of the memory array has a memory controller, element 26". Although each memory bank has a controller 26, it is seen that command decoder 13, refresh address counter 22, address buffer 14, I/O buffer 16, the command input buffer and the clock input buffer are common for all of the banks. That should be contrasted with applicant's Figure 5 in which duplicate circuitry is provided for each bank. Furthermore, claim 11 has been amended to add the substance of claim 12 (now cancelled) and to state that the "processor may simultaneously communicate with more than one of said memory banks." Nakamura, Figure 2, which requires that a substantial number of components be used in common amongst the memory banks, does not anticipate amended claim 11 with its plurality of controllers, row address decoders and column address decoders which enable simultaneous communication with the memory banks. For that reason, it is respectfully requested that the rejection of claim 11, as well as the rejection of its remaining dependent claims 13 - 17, be withdrawn.

In paragraph 12 of the Office action, claim 18 stands rejected in view of Nakamura for substantially the same grounds as the rejection of claim 11. Claims 18 has been amended to make it clear

that each of the memory banks is connected to the processor "independently of the connection of said other memory banks to said processor." It is clear from Nakamura that each of the memory banks is not connected to the processing circuit macro (2) independently of the connection of the other memory banks. That is apparent from Figure 2 in which it seen that each of the memory banks shares command decoder 13, refresh address counter 22, address buffer 14, I/O buffer 16, the command input buffer, and the clock buffer. Thus it cannot be said that each of the memory banks (bank 0, bank 1) is connected to the processor "independently of the connection of said other memory banks to said processor". Accordingly, it is respectfully submitted that the rejection of independent claim 18 as well as the rejection of its dependant claims 19 - 24 should be withdrawn.

In paragraph 13 of the Office action, claim 25 stands rejected in view of Nakamura.. Claim 25 has been amended to recite "each of said memory arrays having a plurality of memory banks, each of said memory banks being connected to said processor independently of the connection of said other memory banks to said processor". The reasons for patentability set forth above with respect to claim 18 are equally applicable to claim 25. Accordingly, it is respectfully submitted that the rejection of independent claim 25, and its dependent claims 26 - 30, should be withdrawn.

In paragraph 14 of the Office action, claim 31 stands rejected as being anticipated by Nakamura. It is the Office's position that:

> The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a "memory controller" shown between the processor and the arrays supplies the same type of circuitry discussed by the applicant as being necessary for the present invention. Simply labeling this circuitry "memory controller" does not teach away from the direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays.

The examiner reads too much into the Nakamura reference. While it is true that the processing circuit macro 2, the memory controller 3, and the SDRAM 4 are shown on the same LSI 1, there is no discussion of the number of traces or circuit routing between these components. It is mere speculation on the part of the examiner that the connection between the processing circuit macro 2 and the SDRAM 4, more particularly the banks in the SDRAM 4, is "direct". In fact, the use of common components in Figure 2 shows that it is not direct. While Nakamura does not discuss the necessity for multiplexing, that silence does not lead to the conclusion that the processing circuit macro 2 is directly connected to the memory banks within the SDRAM 4. A much more likely scenario is that when one bank is busy, access is denied, or delayed, until the read or write operation is completed. The examiner has simply failed to put into the record evidence that Nakamura discloses that which applicant is currently claiming.

Claim 31 has been amended in a manner similar to claim 1. Accordingly, the arguments set forth above for the patentability of claim 1 are equally applicable to claim 31. It is respectfully requested that the rejection of independent claim 31, as well as the rejection of its remaining dependent claims 33 - 36, should be withdrawn.

In paragraph 17 of the office action, independent claim 37 stands rejected under 35 U.S.C. §103(a) in view of Nakamura. It is the examiner's position that

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

It is respectfully submitted that the examiner's position is based entirely on hindsight. It is well settled that there must be some suggestion in the prior art for modifying the prior art to arrive at the claimed invention. There is nothing in the figures which implies simultaneous access. In fact, the figures clearly demonstrate non-simultaneous access in view of the fact that many necessary components such as the command decoder 13, address buffer 14, etc. are common amongst the banks (bank 0, bank 1). There is absolutely no suggestion implied or otherwise for duplicating the common circuitry. For the foregoing reasons it is respectfully submitted that the rejection of independent claim 37, as well as the rejection of its dependent claims 38 - 42 must be withdrawn.

In paragraph 18 of the Office action, claim 43 stands rejected for substantially the same reasons as set forth with respect to claim 37. More particularly, the examiner states "it would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuit for the simultaneous access is shown in Figure 2." It is respectfully submitted that there is no circuitry shown in Figure 2 which enables simultaneous access. To the contrary, while the command decoder 13 is decoding a command, for example, for bank 0, it is not possible for the command decoder to simultaneously be decoding a command for bank 1. Figure 2, rather than showing simultaneous access, shows serial access. Other than the application of hindsight, there is no justification for implying that the circuit of Figure 2 teaches or suggests simultaneous access. Accordingly, it is respectfully submitted that the rejection of independent claim 43, as well as the rejection of its dependent claims 44 - 48, be withdrawn.

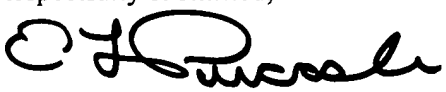
With respect to paragraph 19 of the Office action and claim 49, applicant submits that the Office has not demonstrated, for the reasons set forth above, that Nakamura teaches or even suggests simultaneous access of the individual banks. Accordingly, it is respectfully submitted that the rejection of independent claim 49, and its dependent claims 50 and 51, must be withdrawn.

In paragraph 20 of the Office action, independent claim 52 stands rejected in view of Nakamura. The examiner substantially repeats the argument that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2." Applicant has demonstrated above that there is no circuitry in Figure 2 for enabling simultaneous access. No circuitry is disclosed, and no circuitry is implied other than through the application of hindsight. Accordingly, it is respectfully submitted that the rejection of independent claim 52, as well the rejection of its dependent claim 53 - 58, must be withdrawn.

In paragraph 22 of the Office action, the examiner provides a response to applicant's previous remarks. It is believed that the position as set forth by the examiner in paragraph 22 has been rebutted herein above in dealing with the specific rejections. More specifically, although Figures 1 and 2 of Nakamura do show elements on the same chip, there is no discussion of routing, traces or the like and therefore no indication of how those components are connected. One would expect that those components are connected according to the known methods of the prior art, which do not provide for simultaneous operation as disclosed and claimed in various of the claims. Absent a specific disclosure, the examiner simply cannot assert based on the block diagram of Figure 1 that the components are interconnected so as to provide the simultaneous operation as set forth in certain of the claims. As to the absence of a multiplexer, that cannot be construed to mean that the connection is direct. One would assume that the connection is provided as is common in the prior art rather than according to applicant's novel and unobvious method.

Applicant has made a diligent effort to place the claims in condition for allowance. Accordingly, a Notice of Allowance for claims 11, 13 - 31, and 33 - 58 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicant's attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted,



Edward L Pencoske
Reg. No. 29,688
Thorp Reed & Armstrong LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-7789

Attorneys for Applicant